

TSMC-00-429



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2812
#2/IDS
OKing
8/22/01

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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RECEIVED
JUL 20 2001
TECHNOLOGY CENTER 2890

Subject:

Serial No. 09/845,477 04/30/01

Chine-Gie Lou

A METHOD FOR FORMING SALICIDE
PROCESS

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

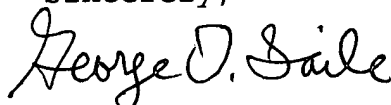
The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,140,216 to Richart et al., "Post Etch
Silicide Formation Using Dielectric Etchback After Global
Planarization", discloses a silicide S/D CMP to expose gate and
Silicide gate top.

The following five U.S. Patents disclose silicide processes:

- 1) U.S. Patent 5,731,239 to Wong et al., "Method of Making Self-Aligned Silicide Narrow Gate Electrodes for Field Effect Transistors Having Low Sheet Resistance".
- 2) U.S. Patent 6,177,336 B1 to Lin et al., "Method for Fabricating a Metal-Oxide Semiconductor Device".
- 3) U.S. Patent 6,162,691 to Huang, "Method for Forming a MOSFET with Raised Source and Drain, Saliciding, and Removing Upper Portion of Gate Spacers if Bridging Occurs".
- 4) U.S. Patent 6,146,994 to Hwang, "Method for Forming Self-Aligned Selective Silicide Layer Using Chemical Mechanical Polishing In Merged DRAM Logic".
- 5) U.S. Patent 6,153,485 to Pey et al., "Salicide Formation on Narrow Poly Lines by Pulling Back of Spacer".

Sincerely,



George O. Saile,
Reg. No. 19572